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What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Invention: taking a processor specification & producing a computer simulation of processor

Specifically: convert a table of opcodes to an architecture description language (ADL) file

Keywords: ADL, HDL, VHDL, nML, LISA, ISDL, opcode

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The New Jersey Machine-Code Toolkit

The New Jersey Machine-Code Toolkit helps programmers write applications that process machine code---assemblers, disassemblers, code generators, tracers, profilers, and debuggers. The toolkit lets programmers encode and decode machine instructions symbolically. Encoding and decoding are automated based on compact specifications. The toolkit is a joint project of Mary Fernández and Norman Ramsey.

You can take a shortcut straight to the source distribution.

There is (old) news for November 1998, as well as really old news. The main news is that you can now download the ML version of the toolkit.

I've started a Toolkit FAQ.

News flash! You can now browse generated decoders on the web!

Mailing lists

To keep up to date with the toolkit, you can send messages to the authors at toolkit@cs.princeton.edu. We also have two mailing lists about the toolkit; toolkit-interest@lists.eecs.harvard.edu goes to people who have expressed some interest in the toolkit, and it carries most general announcements about the toolkit. toolkit-users@lists.eecs.harvard.edu goes to people who are actually using the toolkit, and it carries discussion among users, as well as all the traffic from toolkit-interest. You can subscribe or unsubscribe by putting your email address in this form.

Subscribe   [▣]   to [toolkit-interest ▣]   [Send request]

It's still a good idea to report problems to toolkit@cs.princeton.edu.

Version 0.5 (November 1996)

The toolkit is now in version 0.5. This release is a bugfix release, timed to coincide with the acceptance of our TOPLAS paper. The release fixes many bugs, especially in generated decoders.

- We have added and validated an Alpha specification.

We save release notes from previous versions of the toolkit.

There is no "upgrade path" from earlier versions to 0.5. Get new everything.

ML Version (November 1998)

The ML implementation of the toolkit is distributed "as is," for experimental purposes only.

Distribution

If you think you might want to use the toolkit, a reference manual and source distribution are available. There are annotated specifications (read the report or browse the source directory) for the MIPS, SPARC, Intel Pentium, and Alpha, which show how to use the toolkit to describe real machines. There is also an unannotated specification for the PowerPC 604. Finally there is a toy example that will give you more ideas about how to build applications, and there is a rudimentary disassembler for the SPARC that you may find useful.

Papers

There are two papers describing the main ideas:

- Norman Ramsey and Mary Fernández, The New Jersey Machine-Code Toolkit, *Proceedings of the 1995 USENIX Technical Conference*, New Orleans, LA, January 1995, pp 289-302. [Abstract] [HTML version]. An overview, and the place to begin.
- Norman Ramsey and Mary Fernández, Specifying Representations of Machine Instructions. To appear in *ACM Transactions on Programming Languages and Systems*. [Abstract] [HTML version] This is a comprehensive journal paper that focuses on SLED, the toolkit's specification language.

This paper describes how to test SLED specifications:

- Mary Fernández and Norman Ramsey. Automatic Checking of Instruction Specifications. To appear in the *1997 International Conference on Software Engineering*. [Abstract]

Those who actually want to use the toolkit will probably find the following technical reports useful:

- Norman Ramsey and Mary Fernández, New Jersey Machine-Code Toolkit architecture specifications. Originally Technical Report TR-470-94, Department of Computer Science, Princeton University, October 1994. These annotated descriptions of the MIPS, SPARC, and Intel Pentium show how the toolkit's specification language in action. Highly recommended for anyone planning to write machine descriptions for the toolkit.
- Norman Ramsey and Mary Fernández, New Jersey Machine-Code Toolkit reference manual. Originally Technical Report TR-471-94, Department of Computer Science, Princeton University, October 1994. The manual describes the complete specification language and explains how to use version 0.5.

The toolkit project has also led to a machine-independent method of relocating instructions, described in

- Norman Ramsey, Relocating machine instructions by currying, *Proceedings of the ACM SIGPLAN '96 Conference on Programming Language Design and Implementation*, in *SIGPLAN Notices* **31**, 5 (May 1996), 226-236. [Abstract]

The toolkit's equation solver is described in

- Norman Ramsey. A simple solver for linear equations containing nonlinear operators. *Software---Practice & Experience*, 26(4):467-487, April 1996. An earlier version appeared as Technical Report 95-068, Purdue University, Dept of Computer Sciences, November 1995.

Back to Norman Ramsey's home page.

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| MIMOLA opcode | | Google Search |
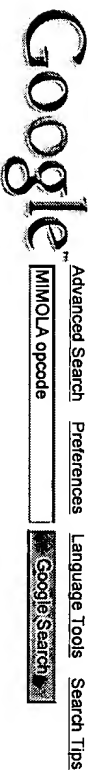
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... for irregular architectures, hard to specify pipelining Structure-Centric ADLs **MIMOLA**,
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... Slide. ASSET Group Seminar, 25/02/2002. http://www.cse.iitd.ac.in/esproject.
MIMOLA (Cont.). Other features. ... (OP_GROUP alu_ops. (**OPCODE** add. (OP_TYPE DATA_OP). ...
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... Insulin. JACOB - **MIMOLA**. LISA. Expression. .... ISA dependent. Simple instruction
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... etc Compiler community: Zephyr, MDES CAD community: **MIMOLA**, CHESS, EXPRESSION ... Specifying
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... is not clear how they generate a cycle- accurate simulator using the **MIMOLA** description. ... ation
of the processor is described in terms of its opcode and operands ...
sigda.org/Archives/ProceedingArchives/Date/ papers/1999/date99/pdffiles/08a_2.pdf - Similar pages

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[PS] **To appear in the Design Automation and Test in Europe (DATE 99) ....**
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... not clear how they generate a cycle-accurate simulator using the **MIMOLA** description. ... operation
of the processor is described in terms of its opcode and operands ...
theory.stanford.edu/~vganesh/date99.ps - Similar pages

[PDF] **Packaging Technology**
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... Attributes. **MIMOLA**. AIDL. nML. ... Normally this would be non-trivial, but since there
is only one instruction in our architecture, no bits are needed for the opcode. ...
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12] since there is no need for separate opcode **tables** and constructors. ...
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... ir = mem[ebus_addr]; pc++ } BC10.control: { pc = (%OPCODE2) } } } LISA and **RADL** have
similar ... mis-prediction can be specified either in the branch **opcode** or in ...
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of the DLX Processor ((**OPCODE OPCODE** ADD ADD ((OPERANDS OPERANDS ...
www.rsp-workshop.org/History/slide03/session-10-p3.pdf - Similar pages

[PDF] TIMA Lab. Research Reports
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... LISA [5] and **RADL** [18] capture VLIW DSP processors. ... (OP_GROUP COPRO_instr (**OPCODE**
VectMul (OPERANDS (_SOURCE_1_ mem) (_SOURCE_2_ mem) (_DEST_ mem) (_LENGTH_ ...
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[PDF] Retargetable Compiled Simulation of Embedded Processors Using a ...
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... The language **RADL** [Siska 1998] is ACM Transactions on Design Automation of ... OPERATION
i_type IN pipe.DC { DECLARE { GROUP **opcode** = { ADDI || ADDUI || SUBI ...
portal.acm.org/ ft_gateway.cfm?id=362662&type=pdf&dl=GUIDE&dl=ACM&CFID=11111111&CFTOKE... - Similar pages

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... **RADL** [16] is an extension of the LISA approach that focuses on explicit support of ... oper-
ation of the processor is described in terms of its **opcode** and operands ...
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... These ADLs include MIMOLA [3] , UDL/I [4] , nML [5] , ISDL [6] , CSDL [34] , Maril
[7] , HMDES [8] , TDL [33] , LISA [9,10] , **RADL** [11] , EXPRESSION [12] and ...
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... But no results are published on simulation speed The language **RADL** Siska is ... Processor
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... ISDL [2], LISA [8], nML [3], EXPRESSION [1], and in- dustry: ARC [4], Tensilica [6],
RADL [12], MDES ... Timing can be specified on a per-**opcode** basis, if necessary ...
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1 Efficient random vector verification method for an embedded 32-bit RISC core

Chang-Ho Lee; Hoon-Mo Yang; Sung-Ho Kwak; Moon-Key Lee; Sanghyun Park; Sangyeun Cho; Sangwoo Kim; Yongchun Kim; Seh-Woong Jeong; Bong-Young Chung; Hyung-Lae Roh;
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on , 28-30 Aug. 2000
Pages:291 - 294

[Abstract]   [PDF Full-Text (396 KB)]   **IEEE CNF**

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http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=hdl+and+opcode%0D%0A%0D%0A%0D%0A....   3/5/04

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1 **An infrastructure for the rapid development of XML-based architecture description languages**
Dashofy, E.M.; van der Hoek, A.; Taylor, R.N.;
Software Engineering, 2002. ICSE 2002. Proceedings of the 24rd International Conference on , 19-25 May 2002
Pages:266 - 276

[Abstract] [PDF Full-Text (1273 KB)] **IEEE CNF**

2 **The use of architecture description languages to describe a distributed measurement system**
Georg, G.; Seidman, S.;
Engineering of Computer Based Systems, 2000. (ECBS 2000) Proceedings. Seventh IEEE International Conference and Workshopon the , 3-7 April 2000
Pages:185 - 193

[Abstract] [PDF Full-Text (148 KB)] **IEEE CNF**

3 **Automatic modeling and validation of pipeline specifications driven by an architecture description language [SoC]**
Mishra, P.; Tomiyama, H.; Halambi, A.; Grun, P.; Dutt, N.; Nicolau, A.;
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and the 15th International Conference on VLSI Design. Proceedings. , 7-11 Jan. 2002
Pages:458 - 463

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

4 **A highly-extensible, XML-based architecture description language**
Dashofy, E.M.; van der Hoek, A.; Taylor, R.N.;
Software Architecture, 2001. Proceedings. Working IEEE/IFIP Conference on , 28-31 Aug. 2001
Pages:103 - 112

[Abstract] [PDF Full-Text (968 KB)] **IEEE CNF**

5 **A survey of architecture description languages**
Clements, P.C.;
Software Specification and Design, 1996., Proceedings of the 8th International Workshop on , 22-23 March 1996
Pages:16 - 25

[Abstract] [PDF Full-Text (862 KB)] **IEEE CNF**

6 **Behavior protocols for software components**
Plasil, F.; Visnovsky, S.;
Software Engineering, IEEE Transactions on , Volume: 28 , Issue: 11 , Nov. 2002
Pages:1056 - 1076

[Abstract] [PDF Full-Text (608 KB)] **IEEE JNL**

7 **A classification and comparison framework for software architecture description languages**
Medvidovic, N.; Taylor, R.N.;
Software Engineering, IEEE Transactions on , Volume: 26 , Issue: 1 , Jan. 2000
Pages:70 - 93

[Abstract] [PDF Full-Text (6816 KB)] **IEEE JNL**

8 **Using the architecture description language MetaH for designing and prototyping an embedded reconfigurable sliding mode flight controller**
McDuffie, J.H.;
Digital Avionics Systems Conference, 2002. Proceedings. The 21st , Volume: 2 , 2002
Pages:8B1-1 - 8B1-17 vol.2

[Abstract] [PDF Full-Text (943 KB)] **IEEE CNF**

9 **Using a software architecture description language to model the architecture and run-time performance of a federate**
Petty, M.D.; McKenzie, F.D.; Qingwen Xu;
Distributed Simulation and Real-Time Applications, 2002. Proceedings. Sixth IEEE International Workshop on , 11-13 Oct. 2002
Pages:85 - 92

[Abstract] [PDF Full-Text (390 KB)] **IEEE CNF**

10 **An XML-message based architecture description language and architectural mismatch checking**
Bo Zhang; Ke Ding; Jing Li;
Computer Software and Applications Conference, 2001. COMPSAC 2001. 25th Annual International , 8-12 Oct. 2001
Pages:561 - 566

11 **Processor-memory co-exploration driven by a Memory-Aware Architecture Description Language**
Mishra, P.; Grun, P.; Dutt, N.; Nicolau, A.;
VLSI Design, 2001. Fourteenth International Conference on , 3-7 Jan. 2001
Pages:70 - 75

[Abstract]   [PDF Full-Text (536 KB)]   **IEEE CNF**

12 **Using the architecture description language MetaH for designing and prototyping an embedded spacecraft attitude control system**
McDuffie, J.H.;
Digital Avionics Systems, 2001. DASC. The 20th Conference , Volume: 2 , 14-18 Oct. 2001
Pages:8E3/1 - 8E3/9 vol.2

[Abstract]   [PDF Full-Text (612 KB)]   **IEEE CNF**

13 **n-SPACE: a formal architecture description language based on process algebra for evolving software systems**
Chaudet, C.; Oquendo, F.;
Automated Software Engineering, 2000. Proceedings ASE 2000. The Fifteenth IEEE International Conference on , 11-15 Sept. 2000
Pages:245 - 248

[Abstract]   [PDF Full-Text (632 KB)]   **IEEE CNF**

14 **Integrating architecture description languages with a standard design method**
Robbins, J.E.; Medvidovic, N.; Redmiles, D.F.; Rosenblum, D.S.;
Software Engineering, 1998. Proceedings of the 1998 (20th) International Conference on , 19-25 April 1998
Pages:209 - 218

[Abstract]   [PDF Full-Text (1348 KB)]   **IEEE CNF**

15 **Scheduling and communication in MetaH**
Vestal, S.; Binns, P.;
Real-Time Systems Symposium, 1993., Proceedings. , 1-3 Dec. 1993
Pages:194 - 200

[Abstract]   [PDF Full-Text (540 KB)]   **IEEE CNF**

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